Title: Design and synthesis of an LDPC decoder for DVB-T2

General Topic: Digital TV, Communication systems, Information theory, Channel coding

Project Start & Duration: beginning of internship may be immediate or upon agreement; the anticipated duration is 6 months

Desirable Knowledge, Skills and Interests:

• Knowledgeable in digital circuit design
• Experience with a digital design tool (RTL design, logic simulation; understanding of basic synthesis and FPGA prototyping)
• Knowledgeable in digital communications theory
• Knowledgeable in signal processing theory
• Paying attention to details, dedicated to deliver a high quality design
• Good communication skills, documentation must be in English
• Programming skills in Verilog, basic C (matlab understanding appreciated)
• Interest in mathematical modeling and simulation of physical systems
• Knowledge of digital TV and DVB specification is useful but not a must

Description:
Abilis and EPFL have started a national research project aiming at the study and the implementation of the DVB-T2 standard.
The DVB-T2 standard is the new standard adopted by DVB whose objective is to drastically increase the transmission capabilities, the services and the robustness of the next-generation digital terrestrial broadcasting system. In this project, a complete DVB-T2 simulator will be developed to study the new algorithms and the main critical blocks.
The candidate will be involved in the design and synthesis of a novel LDPC decoder. The goal of this project is to obtain a parameterizable highly efficiency decoder in terms of silicon area and performance. The student will work with the world leading experts in communications theory and be coached by an expert designer for his day-to-day work.

Internship leaders: Mauro Lattuada and Pierre-Marie Signe